EVALUATION OF THE AGILENT 3458A TIME JITTER PERFORMANCE

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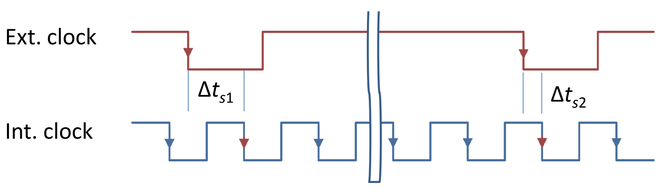
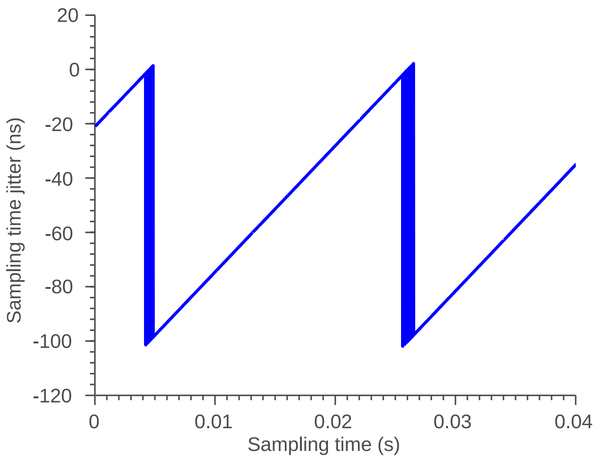
Goal

Determination of time jitter of the Agilent 3458A when external triggering is used at asynchronous two channel sampling

Digital voltmeter sampling timing



External timing jitter error due to finite resolution of internal free running 10 MHz clock in DCV mode. Δt_s can vary from 0 ns to 100 ns.



Slave DMM timing jitter example.
Sampling parameters:
t_s = 10 µs, f_{int} = 100 kHz,
f_{ext} = 100.001 kHz, $t_{j,ext}$ = 2 ns

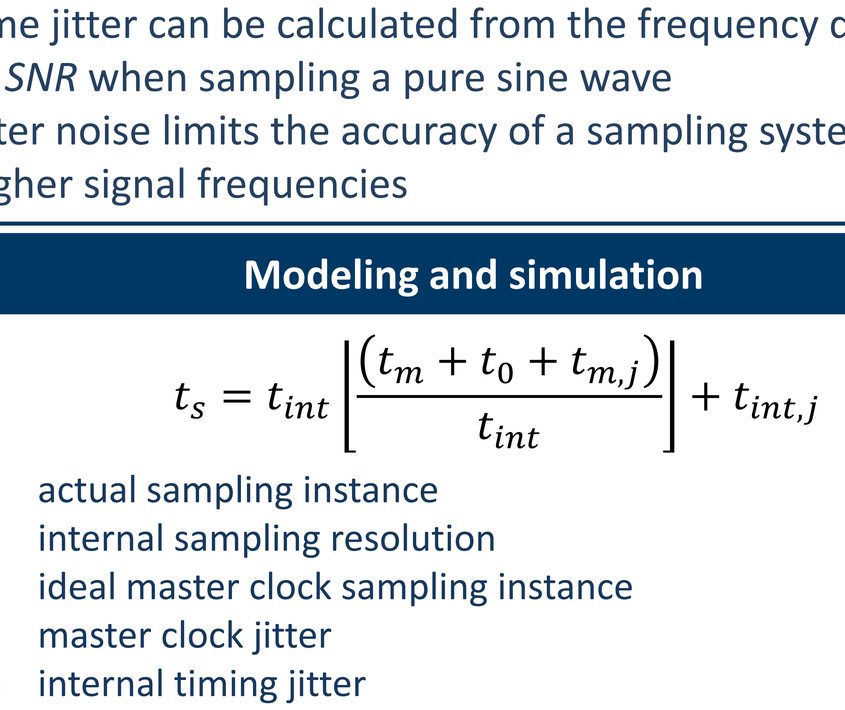
Measuring time jitter

- time jitter or sampling clock noise manifests itself in the amplitude noise whenever the sampled signal changes
- time jitter can be calculated from the frequency dependence of *SNR* when sampling a pure sine wave
- jitter noise limits the accuracy of a sampling system for higher signal frequencies

Modeling and simulation

$$t_s = t_{int}\left\lfloor \frac{(t_m + t_0 + t_{m,j})}{t_{int}} \right\rfloor + t_{int,j}$$

t_s actual sampling instance
t_{int} internal sampling resolution
t_m ideal master clock sampling instance
t_0 master clock jitter
$t_{m,j}$ internal timing jitter
$t_{int,j}$ start timing offset of master clock relative to internal clock

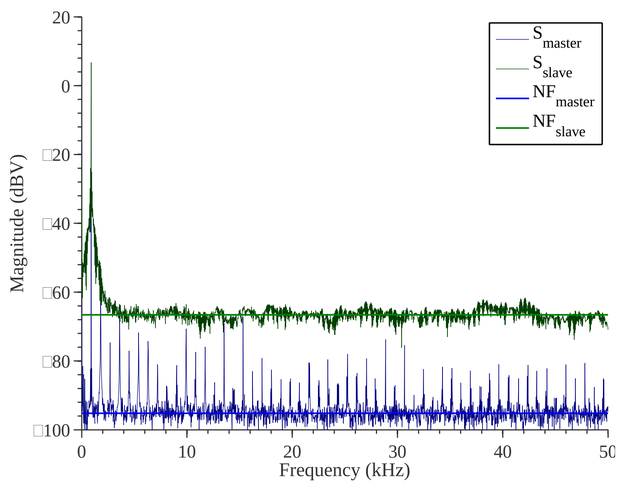


Effective timing jitter as retrieved by simulation around small differences between external and internal clock frequencies
f_s = 10 kHz, t_{int} = 100 ns, $t_{m,j}$ = 450 ps, N = 4000

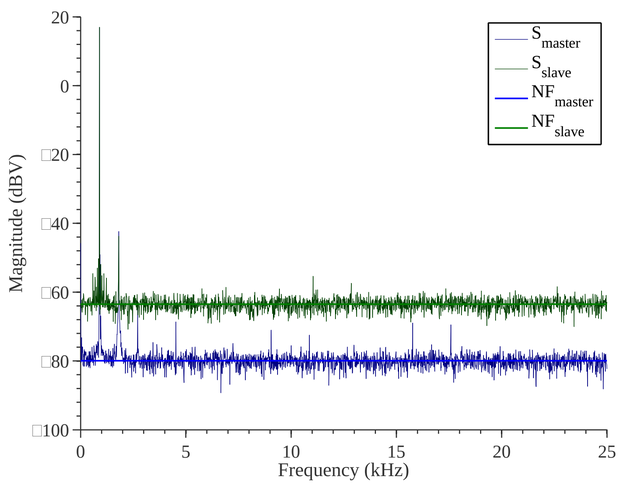
Measurements

- generator Agilent 33522A used in three different setups with one or two DMMs Agilent 3458A
- internal timebase, external generated timebase (using second channel of generator) and two DMMs in master-slave mode
- 4096 samples taken for each measurement
- 10 repetitions made to calculate mean response and standard deviation of measurement result

Results: Jitter spectrum of Agilent 3458A

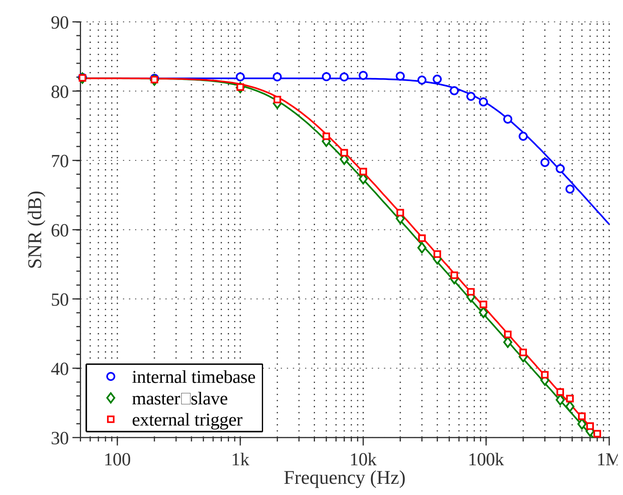


Jitter spectrum (DCV mode)
f = 300.9 kHz, t_a = 1 µs, t_s = 10 µs, U = 7 V

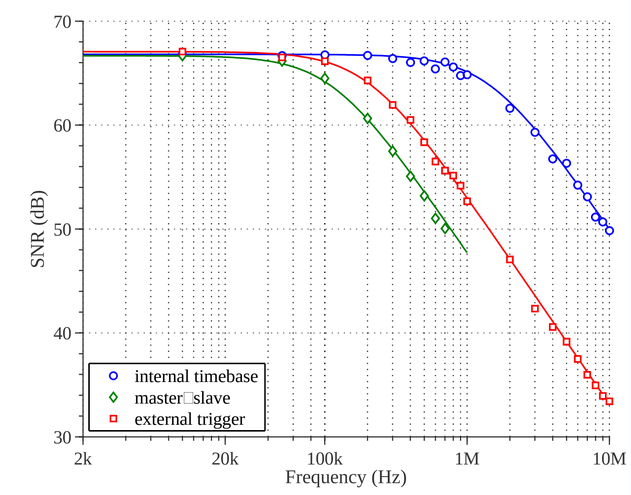


Jitter spectrum (DSDC mode)
f = 1000.9 kHz, t_s = 20 µs, U = 7 V

Results: DCV and DSDC sampled SNR as a function of frequency



DCV sampled SNR
t_s = 10 µs, t_a = 1 µs, U = 7 V



DSDC sampled SNR
t_s = 20 µs, U = 7 V

Results: Measured sampling time jitter with uncertainties

Timebase used	t_j (DCV mode)	t_j (DSDC mode)
Internal	145 ps ± 5 ps	49 ps ± 4 ps
External	6.0 ns ± 0.4 ns	363 ps ± 21 ps
Master-Slave	6.8 ns ± 0.4 ns	660 ps ± 38 ps

Conclusions

- ✓ a sampling voltmeter internal and external time jitter estimated by measuring frequency dependent SNR
- ✓ measured results consistent with the model at frequencies well beyond the input stage filter cut-off frequency
- ✓ master DMM adds approximately 0.8 ns of its own time jitter while triggering the slave DMM
- ✓ effective time jitter for externally triggered DMM remains well below ±50 ns maximum jitter as correctly specified by manufacturer